



UNITED STATES PATENT AND TRADEMARK OFFICE

AM
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,479	10/24/2001	Roger A. Bethard	1376.689US1	5205
21186	7590	06/23/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402-0938			KIM, HONG CHONG	
		ART UNIT		PAPER NUMBER
		2186		
DATE MAILED: 06/23/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/037,479	BETHARD, ROGER A.
	Examiner	Art Unit
	Hong C. Kim	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 24 October 2001.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 is/are pending in the application.
4a) Of the above claim(s) 9-27 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-8 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) 9-27 are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8/12/2004

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

Detailed Action

1. Claims 1-27 are presented for examination. This office action is in response to the application filed on 10/24/02.

Restriction

2. Restriction to one of the following inventions is required under 35 USC § 121:

I. Claims 1-8, drawn to utilizing memory based TLB, classified in Class 711 subclass 207.

II. Claims 9-26, drawn to controlling transfer of block of data, classified in Class 710, subclass 23.

III. Claim 27, drawn to archiving data, classified in Class 714, subclass 2.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions I, II, and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as utilizing memory based TLB, invention Group II has separate utility such as controlling transfer of block of data, and invention Group III has separate utility such as arching data. See M.P.E.P. § 806.05(d).

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and recognize divergent subject matter, and because the searches required for the different groups is not entirely coextensive restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mr. Thomas F. Brennan (Reg. No. 35,075) on June 20, 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-8. Affirmation of this election must be made by applicant in responding to this Office action. Claims 9-27 withdrawn from further consideration by the Examiner, 37 C.F.R. § 1.142(b), as being drawn to non-elected claims.

6. If applicant does not distinctly and specifically point out the supposed errors in the restriction requirement, the election will be treated as an election without traverse (M.P.E.P. § 818.03(a)).

Information Disclosure Statement

7. The information disclosure statement submitted on 8/12/2004 is being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities: The title

of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature.

" a plurality of processing elements", "a plurality of processor translation look-aside buffers for a memory array", and "FIFO memory interface" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Appropriate correction is required.

8. The status of the related U.S. applications must be updated accordingly (e.g., U.S. Patent Application Serial No. #/#/#/# filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number #/#/#/#, filed on December 01, 1990, now abandoned; ...etc.) in the Related Applications section and in any other corresponding area in the specification, if any. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 8, 1, 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaiser et al. (Kaiser) EP0766177A1 in view of Peck, Jr. et al. (Peck) US Paten No. 6,686,920.

As to claim 8, Kaiser discloses an information-handling system (Fig. 1) comprising: a memory (Fig. 2 Ref. 24); and a plurality of processing elements (Fig. 2 Refs. 12's), wherein each of the processing elements is operatively coupled to the memory, wherein the memory includes mapping means for mapping processor addresses received from the processing elements into memory addresses in the memory (Fig. 2 Ref. 220).

However, Kaiser does not specifically disclose wherein the mapping means includes a first mapping function for translating processor addresses associated with a first processing element and a second mapping function for translating processor addresses associated with a second processing element.

Peck discloses wherein the mapping means includes a first mapping function for translating processor addresses associated with a first processing element and a second mapping function for translating processor addresses associated with a second processing element (Fig. 2 Ref. 60a thru 60d) for the purpose of increasing data bandwidth and decreasing the TLB swapping and trashing by distributing TLBs per each PE.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace a single mapping function (processor translation look-aside buffer) of Kaiser with first and second mapping

functions (a plurality of processor translation look-aside buffers) of Peck for the advantages stated above.

As to claim 1, Kaiser discloses an information-handling system, comprising: a plurality of processing elements (Fig. 2 Refs. 12's); and one or more memory sections (Fig. 2 Ref 204 and 24), wherein each memory section comprises: a memory array (Fig. 2 Ref. 24) having a plurality of locations; a memory interface (Fig. 2 Ref. 204) operatively connecting the memory array to each of the processing elements; and a processor translation look-aside buffer, wherein the processor translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements in order to translate addresses received from the processing elements, and wherein the processor translation look-aside buffer has a plurality of entries, the plurality of entries being used to map a processor address into a memory array address of the memory array.

However, Kaiser does not specifically disclose a plurality of processor translation look-aside buffers, wherein each processor translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements in order to translate addresses received from the processing elements, and wherein each processor translation look-aside buffer has a plurality of entries, each one of the plurality of entries being used to map a processor address into a memory array address of the memory array.

Peck discloses a plurality of processor translation look-aside buffers (Fig. 2 Ref. 60a thru 60d), wherein each processor translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements in order to translate addresses received from the processing elements, and wherein each processor translation look-aside buffer has a plurality of entries, each one of the plurality of entries being used to map a processor address into a memory array address of the memory array for the purpose of increasing data bandwidth and decreasing the TLB swapping and trashing by distributing TLBs per each PE.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace a processor translation look-aside buffer of Kaiser with a plurality of processor translation look-aside buffers of Peck for the advantages stated above.

As to claim 4, Kaiser and Peck disclose the invention as claimed above.

Kaiser further discloses I/O processor (Fig. 1 Ref. 120). Peck further discloses the memory sections further include one or more I/O translation look-aside buffers (Fig. 2 Ref. 60c and 60d), wherein each I/O translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements to translate addresses received from the processing element, and wherein each of the I/O translation look-aside buffers has a plurality of entries, each of the entries being used to map an I/O address into a memory array address of the memory array.

As to claim 5, Kaiser discloses 1 method for addressing a memory within a memory system (Fig. 2) comprising: routing a first memory command (Fig. 2 Ref. 210) within the memory system, wherein the first memory command includes a first processor address (Fig. 2 Ref. 12); mapping the first processor address into a first memory address using a mapping function associated with a processor (Fig. 2 Ref. 12); addressing memory data (Fig. 2 Ref. Ref. 24) within the memory system with the first memory address; routing a second memory command (Fig. 2 Ref. 210) within the memory system, wherein the second memory command includes a second processor address (Fig. 2 Ref. 12); mapping the second processor address into a second memory address using a mapping function associated with a processor (Fig. 2 Ref. 12); and addressing memory data (Fig. 2 Ref. Ref. 24) within the memory system with the second memory array address.

However, Kaiser does not specifically disclose mapping the first processor address into a first memory address using a mapping function associated with a first processor and mapping the second processor address into a second memory address using a mapping function associated with a second processor.

Peck discloses mapping (Fig. 2 Ref. 60a thru 60d) the first processor address into a first memory address using a mapping function associated with a first processor and mapping (Fig. 2 Ref. 60a thru 60d) the second processor address into a second memory address using a mapping function associated

with a second processor for the purpose of increasing data bandwidth and decreasing the TLB swapping and trashing by distributing TLBs per each PE.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace a single mapping function of Kaiser with mapping the first processor address into a first memory address using a mapping function associated with a first processor and mapping the second processor address into a second memory address using a mapping function associated with a second processor of Peck for the advantages stated above.

As to claim 7, Kaiser and Peck disclose the invention as claimed above.

Kaiser further discloses I/O processor (Fig. 1 Ref. 120). Peck also further discloses I/O processor (Fig. 2 PCI or AGP I/F).

10. Claims 2, 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaiser et al. (Kaiser) EP0766177A1 in view of Peck, Jr. et al. (Peck) US Paten No. 6,686,920 further in view of Herrell et al. (Herrell) US Paten No. 5,301,287.

As to claim 2, Kaiser and Peck disclose the invention as claimed above.

Kaiser further discloses the memory interface includes a buffer, wherein the buffer accepts memory commands from one or more of the processing elements

and transmits each of the memory commands to the processor translation look-aside buffers.

However, neither Kaiser nor Peck specifically discloses memory interface includes a FIFO.

Herrell discloses memory interface includes a FIFO (col. 7 lines 12-14) for the purpose of providing capability of items in queue or buffer are removed in the same order in which they were added.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace buffer of the combined invention of Kaiser and Peck with FIFO as taught by Herrell for the advantages stated above.

As to claim 3, Kaiser, Peck, and Herrell disclose the invention as claimed above. Peck further discloses Plurality of interfaces. Herrell further discloses a command FIFO (col. 7 lines 12-14).

As to claim 6, Kaiser, Peck, and Herrell disclose the invention as claimed above. Peck further discloses Plurality of interfaces. Herrell further discloses the routing of the first memory command includes processing the first memory command on a first in first out basis with regard to other memory commands (col. 7 lines 12-14).

Conclusion

Art. Unit: 2186

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.
2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).
3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).
4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. Any response to this action should be mailed to:

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner

June 20, 2005

A handwritten signature in black ink, appearing to read "L. J. H. [Signature]".